IARPA-RFI-15-02

Request for Information (RFI): Electronic Design Automation tools for Superconducting Electronics

Synopsis

The Intelligence Advanced Research Projects Activity (IARPA) seeks information on the availability and development of electronic design automation (EDA) tools for superconducting electronics (SCE). This request for information (RFI) is issued solely for information gathering and planning purposes; this RFI does not constitute a formal solicitation for proposals. The following sections of this RFI define the overall scope of the technical domain of interest, along with instructions for the preparation and submission of responses.

Background & Scope

To reach its goal of building a prototype superconducting computer, IARPA's Cryogenic Computing Complexity (C3) program will need to produce superconducting circuits of unprecedented density and complexity [1, 2]. The C3 program will be fabricating circuits using the 10-metal layer, fully planarized process at Lincoln Laboratory [3, 4]. The sophistication of today's complementary metal-oxide semiconductor (CMOS) circuits owes much to a rich set of EDA tools. Superconducting electronic circuit design has unique requirements imposed by superconductivity that prevent repurposing all of the same EDA toolchain used for CMOS design and that require the development of additional tools. The existing EDA toolchain for SCE is currently incomplete and limited in capability [2, 5, 6]. IARPA is interested in learning the best path towards eliminating these deficiencies. Responses should focus primarily but not exclusively on applicability to the IARPA C3 program.

IARPA's short-term goal is to significantly reduce design time, increase the reliability of designs, and enable the design of complex digital circuits with at least 1,000,000 Josephson junctions. The longer-term IARPA goal is to develop a fully integrated EDA toolchain for superconducting digital, analog and hybrid circuits, and bridge the gap between superconducting and CMOS design.

Questions:

- What relevant tools currently exist? What are the opportunities, challenges and limitations associated with adapting CMOS tools for superconducting use? What resources are required?
- Are there aspects of the CMOS development infrastructure other than tools that are important to the maturation of superconducting electronics design?
- What types of tools would be the most effective reducers of design time? What tools would provide the greatest reductions in design risk? Include estimates, if available.

- Are special tools needed for particular types of superconducting electronic circuits (e.g., RSFQ, RQL, analog, hybrid)? What tools are unique to superconducting circuits?

Desirable features:

- Applicable to all families of single flux quantum (SFQ) digital logic
- Work to clock speeds of 100 GHz or greater
- Compatible with an existing CMOS tool chain
- Able to optimize a design based on metrics such as circuit area, power, energy per operation, or speed

Preparation Instructions to Respondents

IARPA requests that submittals briefly and clearly describe the potential approach or concept, outline critical technical issues and obstacles, describe how the approach may address those issues and obstacles and comment on the expected performance and robustness of the proposed approach. If appropriate, respondents may also choose to provide a non-proprietary rough order of magnitude (ROM) regarding what such approaches might require in terms of funding and other resources for one or more years. This announcement contains all of the information required to submit a response. No additional forms, kits, or other materials are needed.

IARPA appreciates responses from all capable and qualified sources from within and outside of the US. Because IARPA is interested in an integrated approach, responses from teams with complementary areas of expertise are encouraged.

Responses have the following formatting requirements:

1. A one-page cover sheet that identifies the title, organization(s), respondent's technical and administrative points of contact - including names, addresses, phone and fax numbers, and email addresses of all co-authors, and clearly indicating its association with IARPA-RFI-15-02;
2. A substantive, focused, one-half page executive summary;
3. Responses to the five questions (limited to 6 pages in minimum 12 point Times New Roman font, appropriate for single-sided, single-spaced 8.5 by 11 inch paper, with 1-inch margins);
4. A list of citations (any significant claims or reports of success must be accompanied by citations, and reference material MUST be attached);
5. Optionally, a single overview briefing chart graphically depicting the key ideas.

Submission Instructions to Respondents

Responses to this RFI are due no later than 4:00 p.m., Local Time, College Park, MD on Friday, February 13, 2015. All submissions must be electronically submitted to dni-iarpa-rfi-15-02@iarpa.gov as a PDF document. Inquiries to this RFI must be submitted to dni-iarpa-rfi-15-02@iarpa.gov. Do not send questions with proprietary content. No telephone inquiries will be accepted.

Disclaimers and Important Notes

This request for information (RFI) is issued solely for information gathering and planning purposes; this RFI does not constitute a formal solicitation for proposals. Respondents are advised that IARPA is under no obligation to acknowledge receipt of the information received, or provide feedback to respondents with respect to any information submitted under this RFI.

The responses to this RFI may be used to help in the identification of promising areas for investment through vehicles such as programs or small studies, as well as in the planning of an agenda and participant list for a potential workshop on EDA tools for superconducting electronics. If appropriate, a separate workshop announcement may be posted at a later date with additional details.

Responses to this notice are not offers and cannot be accepted by the Government to form a binding contract. Respondents are solely responsible for all expenses associated with responding to this RFI. IARPA will not provide reimbursement for costs incurred in responding to this RFI. It is the respondent's responsibility to ensure that the submitted material has been approved for public release by the information owner.

The Government does not intend to award a contract on the basis of this RFI or to otherwise pay for the information solicited, nor is the Government obligated to issue a solicitation based on responses received. Neither proprietary nor classified concepts nor information should be included in the submittal. Input on technical aspects of the responses may be solicited by IARPA from non-Government consultants/experts who are bound by appropriate non-disclosure requirements.

References

[1] http://www.iarpa.gov/index.php/research-programs/c3

[2] D. S. Holmes, A. L. Ripple, M. A. Manheimer, “Energy-efficient superconducting computing—Power budgets and requirements,” *IEEE Trans. Appl. Supercond.*, vol. 23, no. 3, pp.1701610, 2013. DOI: 10.1109/TASC.2013.2244634

[3] Sergey K. Tolpygo, Vladimir Bolkhovsky, Terence J. Weir, William D. Oliver, Mark A. Gouker, “Fabrication Process and Properties of Fully-Planarized Deep-Submicron Nb/Al-AlOx/Nb Josephson Junctions for VLSI Circuits,” *IEEE Trans. Appl. Supercond.*, 2014. DOI: 10.1109/TASC.2014.2374836

[4] Sergey K. Tolpygo, Vladimir Bolkhovsky, T.J. Weir, C.J. Galbraith, Leonard M. Johnson, Mark A. Gouker, Vasili K. Semenov, “Inductance of Circuit Structures for MIT LL Superconductor Electronics Fabrication Process with 8 Niobium Layers,” *IEEE Trans. Appl. Supercond.*, 2014. DOI: 10.1109/TASC.2014.2369213

[5] C. J. Fourie, M. H. Volkmann, “Status of superconductor electronic circuit design software,” *IEEE*

Trans. Appl. Supercond., vol. 23, no. 3, p. 1300205, Jun. 2013. DOI: 10.1109/TASC.2012.2228732

[6] L.C. Mueller, C.J. Fourie, “Automated State Machine and Timing Characteristic Extraction for RSFQ Circuits,” *IEEE Trans. Appl. Supercond.*, vol. 24, no. 1, pp. 1300110, Feb. 2014. DOI: 10.1109/TASC.2013.2284834